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Contracts Management Office (CMO)
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Attention: Mr. Douglas M. Pollock

Subject: Contract No. MDA972-93-C-0057; GTEL Project No. 852
Quarterly Technical Report (SLIN 0002AB)

Dear Mr. Pollock:

GTE Laboratories Incorporated hereby submits the subject report covering the period February 23, 1994 through May 23, 1994, in accordance with the terms of the Contract.

If you should have any questions or require any additional information or further clarification, please contact me at (617)466-2954.

Sincerely,

Linda Rossi
Contracts Administrator

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During the third quarter of the CORD project progress was made in the area of design and development of the various subunits of the system. Test and evaluation of the functional blocks built during the past quarter was the focus of the system group at Stanford University and the optoelectronics group at GTE Laboratories. Detailed performance estimates were made with respect to signaling and its interference with the information channel. Progress was also made in the construction of the CRO module with detailed evaluation of the WDM components to be used and completion of the development of the high speed header detector module. Development of the logic control for CORD's contention resolution strategy was pursued further. Moreover, a "Multi-Packet" CORD architecture was developed and shown that it can substantially reduce the packet loss probability. Logic control design was then provided also for this improved version of the CORD.

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1. CONSORTIUM EXECUTIVE SUMMARY

During the third quarter of the CORD project the consortium continued its effort in subsystem development and construction. Many functional blocks were built, tested and evaluated. Also evaluated were electronic and optical units purchased from vendors. No surprises were found so far in the performance of these devices or components. Delays in delivery however, will affect somewhat the scheduling although so far not too seriously. Delay in fabrication of the digital optical switch may have a scheduling effect down the road, but the extent of this delay is still not clear.

Work at GTE Laboratories involved completion of the header detector module comprised of a high speed, surface mounted photodetector and a planar waveguide directional coupler. This module has been characterized in terms of its performance and speed of operation. initial results show about 5 GHz bandwidth, which is well suited for detection of the highest subcarrier (3.5 GHz). Fabrication of the optical amplifier package has been completed and the package is being assembled. Initial tests show excellent fiber alignment stability over time and this task is expected to be completed shortly. The optical switch development requires refinement of the waveguide geometry to avoid multimode operation. This multimode operation is believed to be the reason for insufficient extinction ration observed in the X-type switches.

At Stanford University we have continued our design and development of the prototype and sub-systems. In particular, we completed and evaluated the performance of the payload data and header transmitters and receivers, and packaged, tested and characterized the lasers and photo-detectors. We also built and tested the circuitry required for header channel clock recovery and continued the design of the data traffic generation and recovery logic sub-systems. Experimental time domain eye diagrams and frequency spectra of the header and payload data channels were taken with the signal power at ratios optimized by simulation and theoretical calculations. Crosstalk between the payload data and header channels has been alleviated by the use of prefiltering. Measurements have been taken to evaluate the effect of different prefiltering techniques on both the received payload data and header channels.

The 80 Mbps header channel Delay-line Phase Alignment (DPA) circuit has been built and tested. It is used to recover the header channel clock in only a few bits. Special care has been taken to improve the reliability of the DPA. This will ensure proper operation despite the non-uniformity of the multi-tap delay-lines, clock oscillator frequency drift, and signal noise or waveform distortion.

The chip-set, used to convert the 2.488 Gbps serial payload data traffic to parallel format, has been received for the data transmitter and receiver portions of the prototype. Initial circuits are being built to verify the performance of the chip-set. We have established a technical point of contact with the manufacturer for aid in developing circuits with this recently available chip-set. A limiting amplifier, needed to stabilize the power level of the incoming payload data signal has been chosen and ordered.

The circuitry required for the inter-node slot synchronization has been designed. The "ping" detector components have arrived and are currently being assembled. The high level design of the traffic generator / detector and performance monitor logic has been completed and a PLD family with sufficient performance selected.

The focus of UMass activity during the third quarter period has been the development of the logic control for CORD's electronic control. In addition to designing a solution for the design proposed originally, UMass developed a "Multi-Packet" CORD architecture and showed that it can substantially reduce the packet loss probability. Logic control design was then provided also for this improved version of the CORD. The following specific tasks were completed within this time frame: Control logic which will be used to design the control electronics for the original two stage CORD testbed Multi-Packet architecture for CORD which improves packet loss probability, while maintaining the original two stage design Comment: The Multi-Packet architecture can work with the control logic designed for the originally proposed CORD generalized control logic for the Multi-Packet architecture which further improves system performance.

For a successful demonstration of the CORD approach, an optimal control logic can efficiently drive the switches of the Contention Resolution Optic (CRO). This operation is performed on the basis of the information available at the node. This consists of arriving packets detected with the Subcarrier Signaling and packets arrived in previous time slots and stored in CRO. The elaboration of this information must be simple, and effected within the given time interval available in a slot (approximately 200 ns). Three different cases consisting of a Control Logic and CORD architecture have been elaborated for the testbed during this effort.

The same Control logic applied to a Multi-Packet architecture developed by UMass during the preceding quarter designed to improve packet loss properties of the network, while maintaining the two stage design improved control logic for the Multi Packet architecture as well further reducing the packet loss probability. In designing the Control Logic two aspects have been considered as central to the design:

a) the optimality of the (FIFO) reception strategies, and

b) the advantages of the (Multi Packet) Delay Line architecture.

Further details on both above aspects were given in the Second Quarterly Report issued by UMass.

First control configuration: In this configuration, one slot Delay Lines (DLs) are used, consistent with the original CORD design. The control strategy is derived from the original FIFO receiver Quadro control, and is designed to solve contention in CORD based on the information consisting of the identity of the arriving packets and of the packets stored in the two DLs.

Second control configuration: In the second configuration DLs can be Multi-Packet DLs, i.e., each DL can be several slots long. Strategy A1 is used to control this second configuration of CORD. Hence, strategy A1 can be used in either the first or the second configuration without modifications. The information used by A1 consists of the identity of the arriving packets and of the two packets currently leaving the two DLs. Note that the identity of the other packets stored in the Multi-Packet DLs is not considered by the control strategy.

Third control configuration: The third configuration deals with Multi-Packet DLs. A different strategy, A2 is proposed for this configuration taking into account the Multiple Packets per slot property of the CORD. This second strategy makes use of the information consisting of the identity of the arriving packets, the identity of the two packets currently leaving the two DLs and the identity of the packet stored in one of the two Multi-Packet DLs which is not leaving the DL in the current slot.

A comprehensive comparison between these three configurations under different DLs lengths (where possible) was carried out during this period. It shows 1) a significant improvement

obtained by the Multi-Packet DL approach versus the original single packet DL approach and 2) advantages in using strategy A2 versus strategy A1. Sizing study for the Multi-Packet approach was also completed, revealing an optimal design for DLs length in the two stage CORD. Choice of the control strategy will be made shortly based on its implication with regard to component availability, and the amount of changes in the original plan needed.

The UMass team is currently working on achieving new results for the distributed design and the adaptation of the original Quadro to improve performance in ring topologies. An analytical model is also under development to allow a more complete evaluation of the performance achieved by this new approach. In parallel, a detailed study and analysis on the Multi-Packet architecture is being carried out. The following list provides a partial description of the main efforts for the next quarter at the UMass networking laboratory: Definition of strategies for Multi Receiver Quadro in stations requiring large amount of data exchange, which exceeds the single channel data rate. Study of the physical layer software module, suitable for optical and all-optical networks description and simulation. Definition of the software interface with the already existing simulator tools developed at UMass, i.e., CONSIP and ETS. Analytical modeling of Quadro distributed strategies in ring topologies Analytical modeling of the Multi-Packet length DL approach for CORD.

The section below contains the technical report of GTE Laboratories only. Stanford University and University of Massachusetts will submit their reports separately.

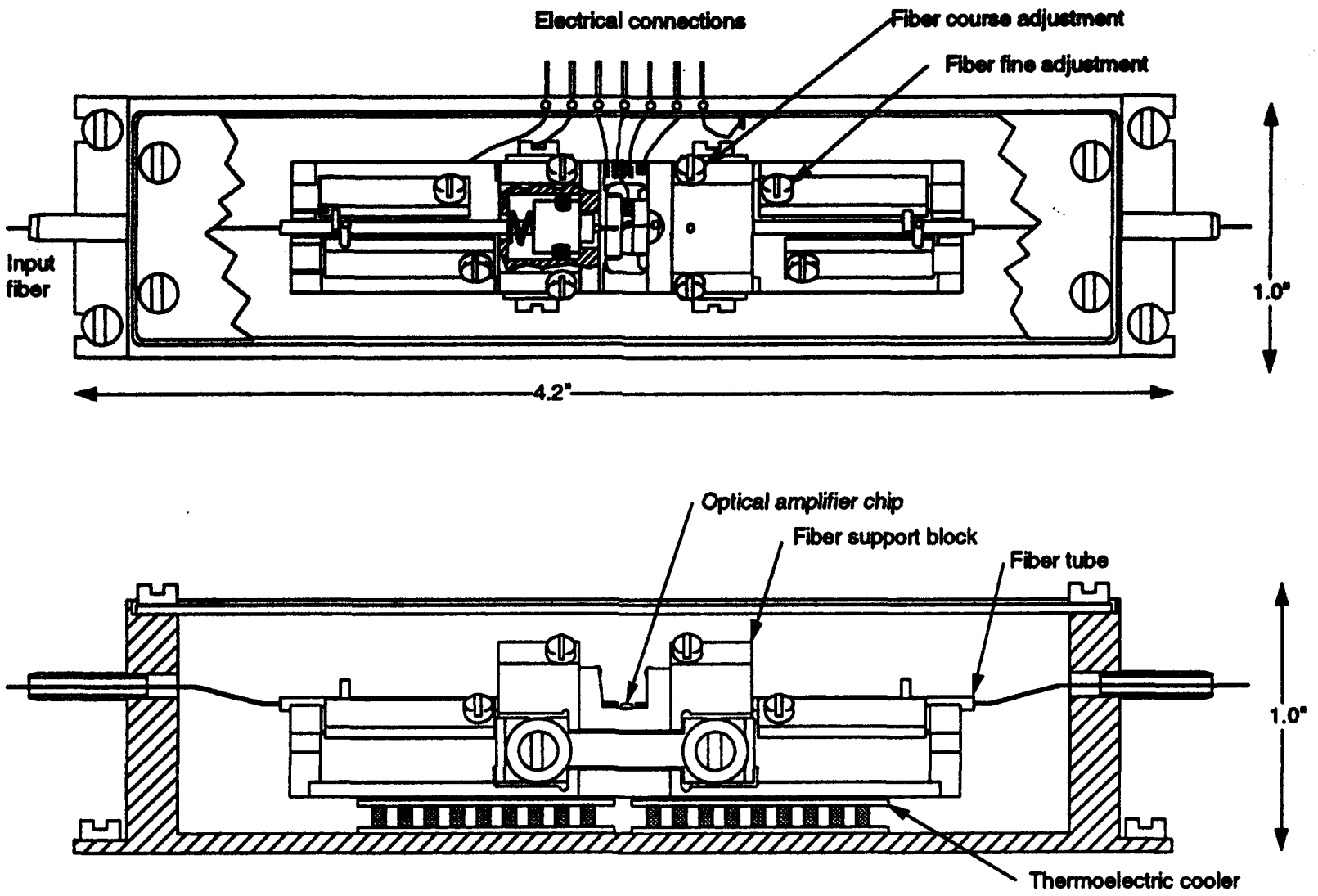
1. TECHNICAL SUMMARY

1.1 AMPLIFIER PACKAGING

A new optical amplifier package design has been completed, parts have been fabricated and package assembly has begun. Earlier package designs, in which the optical fibers were held in place with low-melting-temperature solder, exhibited fiber alignment drift with time. This eventually rendered the device unusable, since these packages could not be repaired. The new design incorporates a mechanical fine-position adjustment for each fiber as part of the package. It will now be possible to realign the fibers should drift occur. A prototype of the alignment mechanism has been tested and has shown good stability and control of fiber position.

A drawing of the complete amplifier package, including the fiber alignment mechanism and enclosure, is shown if Fig. 1. The fiber is bonded inside a metal tube which is supported by a block having course and fine alignment mechanisms. The fine adjustment, through a series of levers, reduces the adjustment screw motion by a factor of 100, so that one turn results in 3 μm of motion at the fiber tip. This is sufficient to achieve the required alignment accuracy of 0.2 μm.

Input and output fiber alignment mechanisms are attached to opposite faces of a block holding the optical amplifier chip and the entire assembly is mounted on a thermoelectric cooler in an enclosure. The enclosure has a removable cover to allow fiber adjustments, if necessary.


Electrical connections
Fiber course adjustment
Fiber fine adjustment
Input fiber
1.0"
4.2"
Optical amplifier chip
Fiber support block
Fiber tube
1.0"
Thermoelectric cooler

Amplifier chips for this package have been mounted and tested. Some devices are available with fiber-to-fiber gains as large as 20 dB. Assembly of the first units in this package should be complete by the end of May.

1.2 WAVELENGTH DIVISION MULTIPLEXERS

Two Wavelength Division Demultiplexing devices were received from JDS-Fitel and were characterized at GTE. These devices were designed to operate at the wavelengths of 1308/1320 nm. The spectral response was measured by using an 1.3 μm LED as a broad light source and a spectrometer to select particular wavelengths. Figures 2 & 3 show the spectral responses of these two devices designated as WD1313U-AZM1308 and WD1313UA18M1308 respectively. The characteristics of both WDMs are almost identical. The results indicate that this type of demultiplexer provides sufficient isolation in the wavelength ranges of 1306 to 1314 nm for one channel with second channel centered at 1290 to 1300 nm or 1320 to 1330 nm.

An 1308 nm DFB laser diode was used to measure the insertion losses and the extinction ratios of these WDMs at λ = 1308 nm. The results for both WDMs are also almost identical. The insertion loss from common channel to channel 1308 at λ = 1308 nm is under 1.0 dB. The extinction ratio between channel 1308 and channel 1320 at λ = 1308 nm is over 21 dB. These insertion loss and extinction ratio are polarization independent.

The back reflections of these WDMs were measured by using a Hewlett Packard 8504A Precision Reflectometer. These WDM devices have very low back reflections. Figure 4 & 5 show the back reflections of WD1313U-AZM1308 and WD1313UA18M1308 are -58.38 dB and -60.43 dB respectively.

Figure 2 : Spectral Response of WD1313U-AZM1308, S/N Y8757

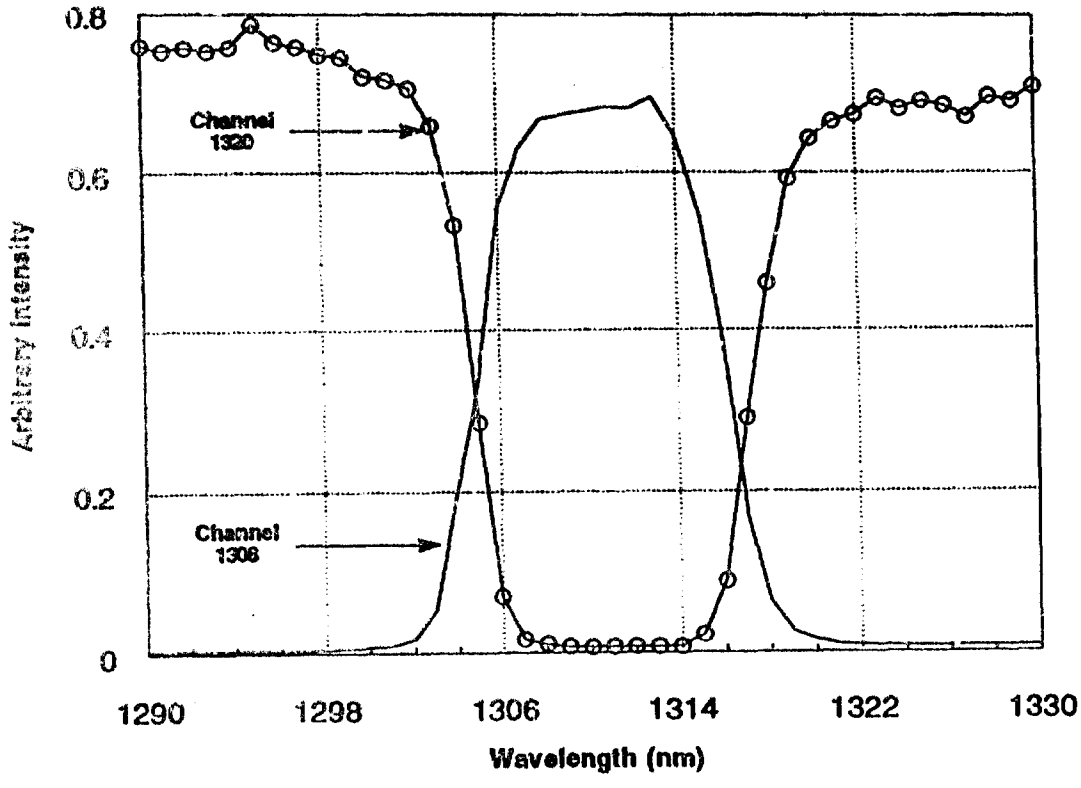


Figure 3 : Spectral Response of WD1313UA18M1308, S/N Y8756

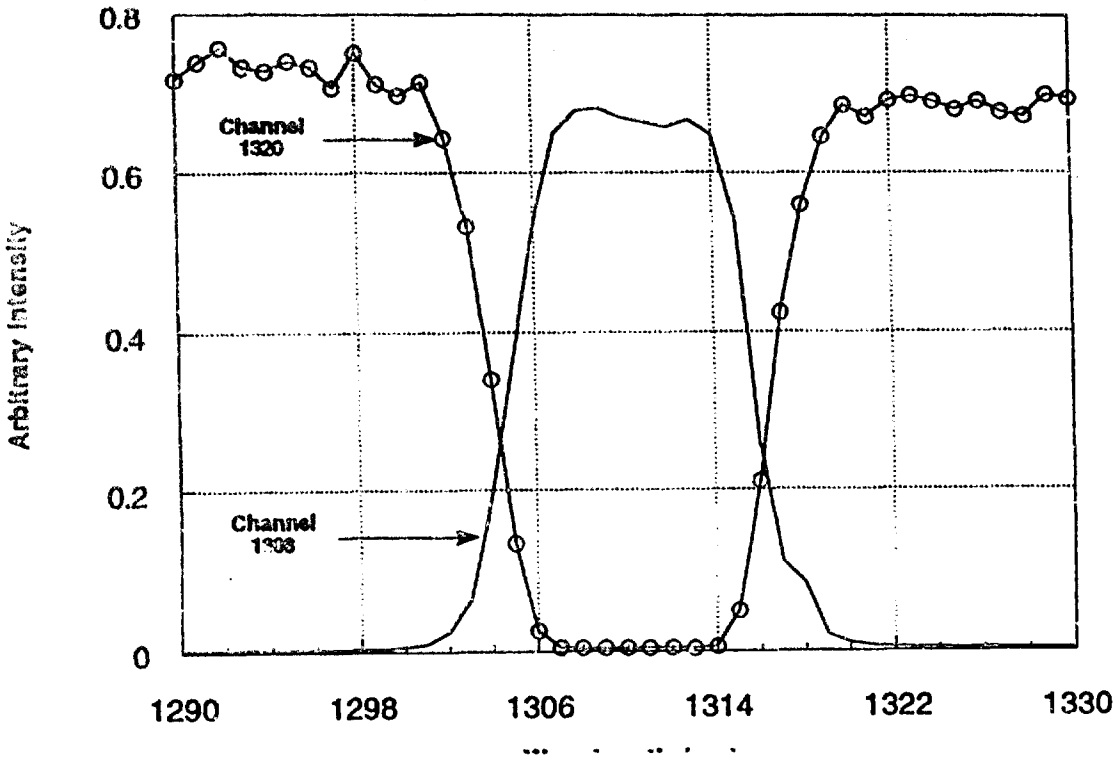


Figure 4 : Back Reflection of WD1313U-AZM1308, S/N Y8757

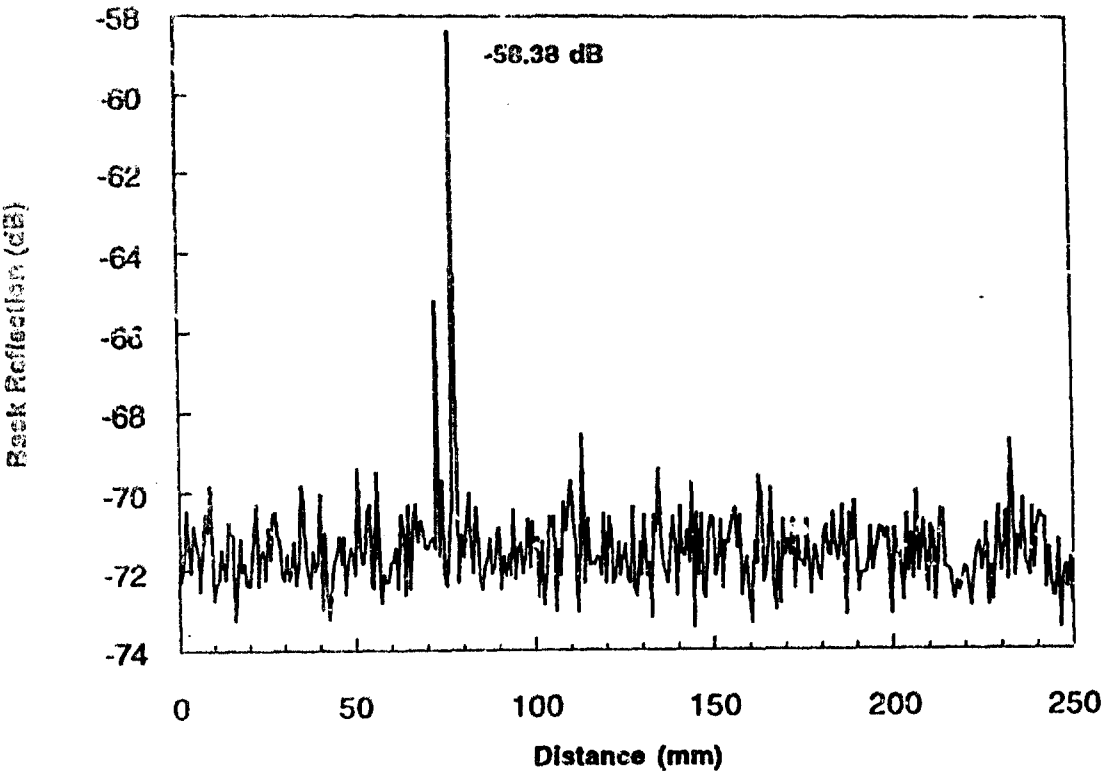
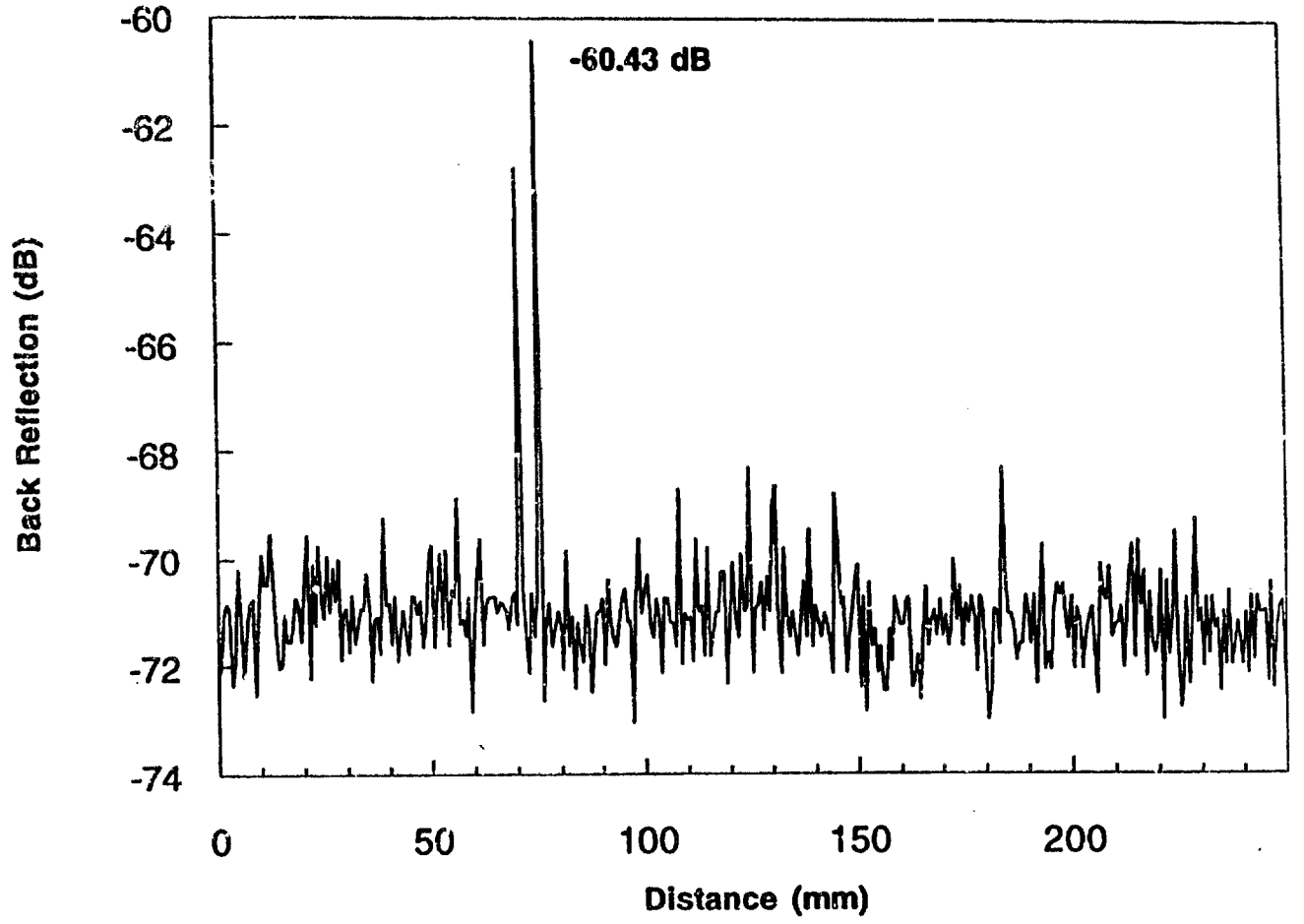


Figure 5 : Back Reflection of WD1313UA18M1308, S/N Y8756



1.3 OPTICAL SWITCH

This quarter's milestone for fabrication of a 2x2 digital optical switch with extinction ratio greater than 20 dB is being delayed by two quarters. While excellent results were achieved with 1x2 switches, as shown by record extinction ratios, progress has been much slower for 2x2 switches. The primary problem is the presence of higher order transverse spatial modes. Although the fundamental mode usually switched, the higher order mode did not. This is consistent with our modeling, which shows that the higher-order mode has a much larger step index. The fraction of light injected into the unswitchable higher-order mode thus severely limited the extinction ratio.

A study was launched to determine why the switches do not operate in a single spatial mode. First, a large number of test waveguides was characterized to determine the effect of varying dimensions and processing procedures. The modal characteristics were not affected by fabrication processes (such as the addition of nitride or metalization), and therefore presumably the problems are not a result of fabrication-induced stress. However, the modal

characteristics did depend slightly on waveguide length. Longer chips less were prone to higher order modes, as consistent with higher propagation losses for the higher order mode. This observation is the basis for the plan described below to "strip" the higher order modes in order to increase the switch extinction ratio.

Two approaches are being immediately pursued in fabricating new 2x2 switch wafers:

(1) We are now processing switch wafers with a combination of ridge width (5.0 μm) and guiding/cladding layer thicknesses which successfully produced singlemode waveguides in earlier tests, and is considered a good candidate for single-spatial-mode switches.

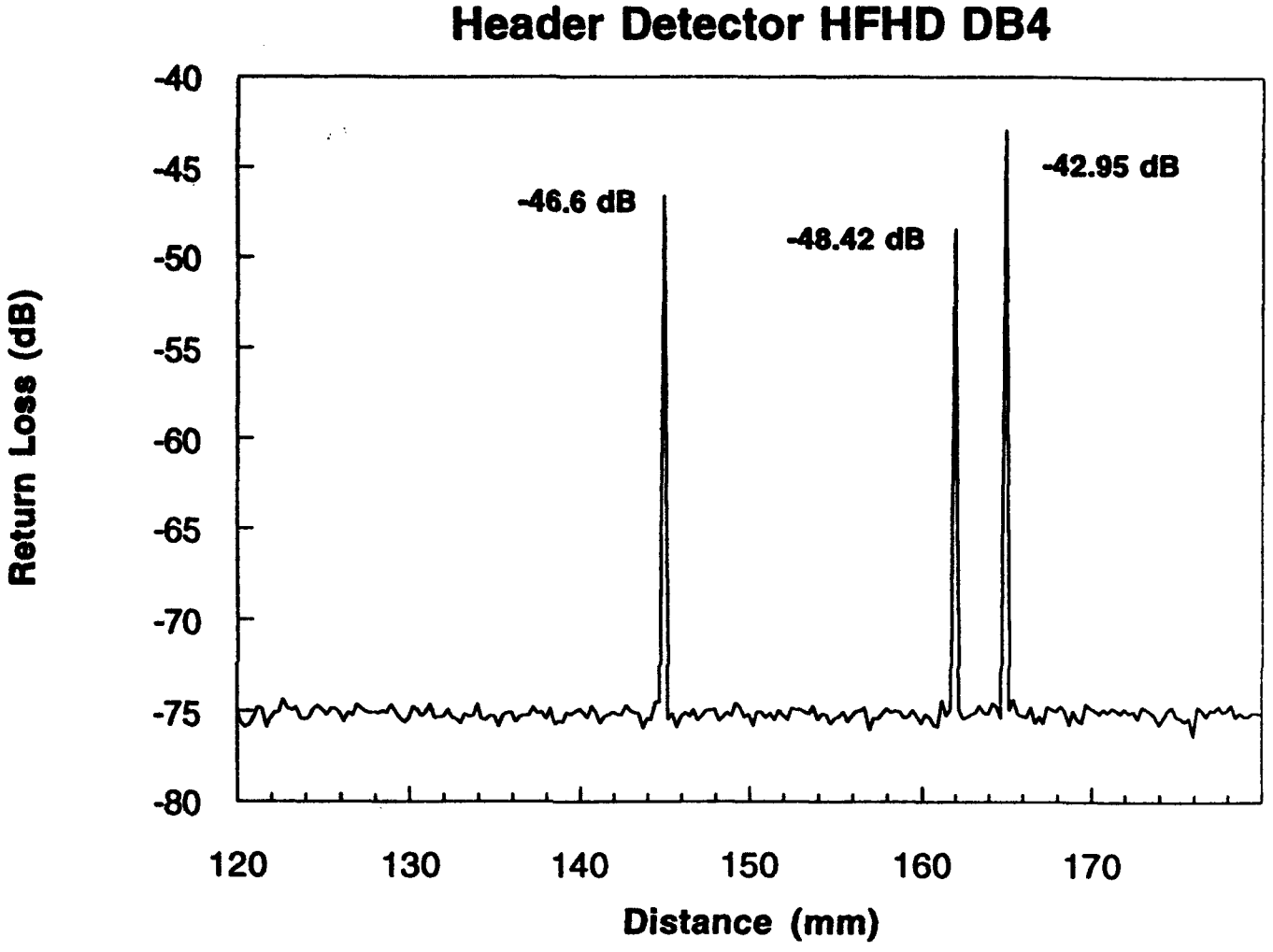
(2) We plan to take advantage of the demonstrated difference in loss between the fundamental and higher-order modes to "strip" the higher-order mode out of the waveguide. To this end, we have designed a new, longer test-structure mask which incorporates curved waveguides as planned for the packageable 2x2 switch. These longer test structures will permit a more accurate measurement of the differential loss, as well as the selective loss of higher order modes in the curved waveguides. Accurate loss measurements were not possible in our previous switches, due to their short length (~ millimeter), but measurements suggest losses on the order of 1 dB/cm for the fundamental mode and 30 dB/cm for the higher-order mode. This information will be used to design a switch which strips out the higher-order mode, and therefore operates in a single spatial mode with high extinction ratio.

Finally, a more rigorous model will be used to refine the switch design and identify a parameter space where the switches are less sensitive to variations in growth and fabrication parameters (such as layer thickness and composition and ridge width). The limitations of the previous model have been reached, as verified by measurements of the near field beam profile. These measurements reveal a triangular symmetry, which cannot be explained by our one-dimensional effective index approximation. For this purpose, we have contracted with the University of Waterloo to perform an exact, two-dimensional modeling analysis (using internal GTE funding).

This plan of action covers changes in switch design from two perspectives: (1) responding to previous empirical results, and (2) improved modeling. Implementation of this plan will cause a delay estimated at four months in the milestone for demonstrating a 2x2 switch with a 20 dB extinction ratio, although initial 2x2 switches may be achieved earlier.

1.4 HEADER DETECTOR

The header detector module has been fabricated and its assembly completed. It is mounted in a high speed package using ceramic strip lines and SMA connector to the outside. Its frequency response extends out to 5 GHz. Back reflection due to fiber-waveguide characteristics are shown below in figure 6. The first two peaks correspond to reflections by the fiber waveguide interface. The third peak is due to the detector end of the waveguide.



2 MILESTONES

This quarter milestone to demonstrate a 2x2 digital optical switch is being delayed till September due to insufficient extinction ratio in the present samples. The reason for this is that the waveguides used in fabrication of the switch turned to support more than one mode and therefore impair the switch performance. A more precise modeling and geometry will be used in the next iteration to limit the guides to single mode operation and provide the switching characteristics needed.